

PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION  
International Bureau



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 :

G06F 13/00

A2

(11) International Publication Number:

WO 00/17759

(43) International Publication Date:

30 March 2000 (30.03.00)

(21) International Application Number: PCT/GB99/03089

(22) International Filing Date: 16 September 1999 (16.09.99)

(30) Priority Data:

9820430.8	18 September 1998 (18.09.98)	GB
9820428.2	18 September 1998 (18.09.98)	GB
9820412.6	18 September 1998 (18.09.98)	GB
9820410.0	18 September 1998 (18.09.98)	GB

(71) Applicant (for all designated States except US): PIXELFUSION LIMITED [GB/GB]; 2440 The Quadrant, Aztec West, Almondsbury, Bristol BS32 4AQ (GB).

(72) Inventors; and

(75) Inventors/Applicants (for US only): PHELPS, Richard, Carl [GB/GB]; 13 Oxbarton, Stoke Gifford, Bristol BS34 8RP (GB). WINSER, Paul, Anthony [GB/GB]; 32 Epsom Close, Downend, Bristol BS16 6ST (GB).

(74) Agent: HASELTINE LAKE & CO.; Imperial House, 15-19 Kingsway, London WC2B 6UD (GB).

(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published

Without international search report and to be republished upon receipt of that report.

(54) Title: APPARATUS FOR USE IN A COMPUTER SYSTEM

(57) Abstract

Apparatus for use in a computer system comprises a bus architecture, a plurality of modules connected to the bus architecture, at least one module being latency tolerant and at least one module being latency intolerant. The bus architecture comprises a primary bus (3) having latency intolerant modules connected thereto, a secondary bus (4) having latency tolerant modules connected thereto, and a primary to secondary bus interface module (5) interconnecting the primary and secondary buses.